TEMPERATURE VARIATION EFFECTS IN NANO-MOSFETS BASED ON SIMULATION STUDY

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Abstract
A numerical simulation study on double-gate (DG) nano-MOSFET has been investigated in this paper. The objective of this study focuses on effects of temperature variation upon the electronic and transport properties in nano-MOSFETs. In this study, electrical characteristics such as electron density, average electron velocity, electron mobility and current-voltage (I-V) are analyzed. The scope of this study covered low temperature range to high temperature range (77 K to 500 K). Numerical simulations are then performed to investigate the influence of temperature variation on electron transport properties in Silicon (Si) channel of DG nano-MOSFETs at nanoscaled dimension. The outcome of this study is to verify and determine a suitable DG nano-MOSFET design which can be used for low temperature to high temperature applications.

Keywords: double-gate nano-MOSFET, temperature, electronic transport

1. Introduction

Silicon (Si) based semiconductor devices have been used in severe environments such as in very low temperature ranges, very high temperature ranges and high radiation environments. This study is focusing to understand the effects of temperature variation in nano-MOSFETs based on simulation results and analysis. Analytical electron transport models for fully depleted (FD), doubled-gated (DG), n-MOSFETs which include the effects of temperature variation in Silicon channel materials have been used in this simulation [1,2]. The temperature range of interest is between 77 K and 500 K. The effects of very low and very high ambient temperatures on the electrical characteristics have been studied. The effects of temperature variations on the threshold voltage, electron mobility, leakage current, on-state current, average electron velocity and electron density distribution have been analyzed.

The nano-MOSFET device characteristics and circuit behaviour that changes with the variation in temperature can be predicted and simulated with suitable models [3,4]. The study of severe operating temperatures of nano-MOSFETs is important for selecting suitable attractive materials for low power, low temperature, high power, high temperature and radiation tolerant applications of analogue and digital circuits. This could lead to significant savings in cost and space

in packaging and cooling systems for industrial process controls including hybrid electric vehicles, aircraft industries, the geothermal and mining explorations and space exploration industries. MOSFETs are widely used in amplifier design, analogue integrated circuits (ICs), digital CMOS design, power electronics and switching devices. Diodes and MOSFETs are used as switching devices in dc-dc converters and ac drives which are extensively used in power electronics, power systems, traction drives and hybrid electric vehicles. This study could enable nano-MOSFETs to be utilized in some of the above mentioned industrial applications.

2. Overview of the Device Design and Mobility Modelling

Figure 1 shows the essential physical structure of nano-MOSFET that has been used in this study.

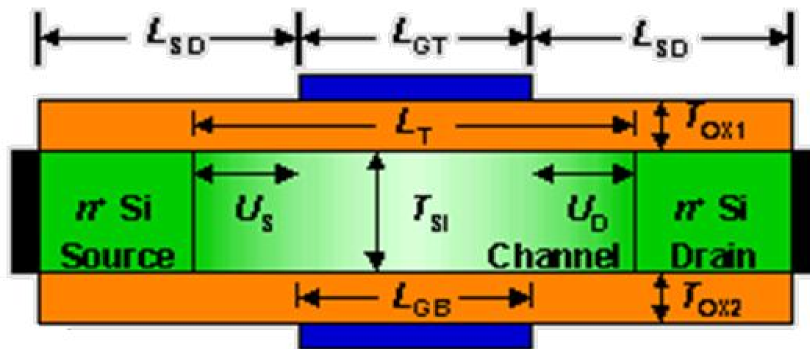

Figure 1: Physical structure of double-gate nano-MOSFET used in temperature effects simulation.

The source and drain terminals are heavily n^+ doped with either arsenic or phosphorus at $1x10^{20}$ cm^{-3}. The channel material used is Si. The channel body doping is intrinsic. The Si channel thicknesses (T_{Si}) is fixed at 1.5 nm for different temperatures studied. Symmetrical top gate length (L_{GT}) and bottom gate length (L_{GB}) are fixed at 10 nm. The source overlap (U_S) and drain overlap (U_D) are zero. The source and drain length (L_{SD}) are both 7.5 nm whereby they have to be the same. Top insulator thickness (T_{OX1}) and bottom insulator thickness (T_{OX2}) are both 1.5 nm. The top and bottom dielectric materials are SiO_2. The top and bottom gate contact work function are fixed at 4.188 eV with Aluminium gate material.

The following specific issues will be addressed in this paper :

1) 2D electron density along the channel
2) Average electron velocity along the channel
3) Drain current versus gate voltage characteristic
4) Ambient temperature variation

To examine these effects, nano-MOSFET model shown in Figure 1 has been numerically simulated using nanoMOS 3.5 simulation software. Three electron transport models have been examined :- (1) ballistic transport using Green's function approach, (2) ballistic transport using semiclassical approach, and (3) drift diffusion approach. All these three transports are essentially one-dimensional type.

In simulating drift diffusion electron transport model, the popular Caughey-Thomas doping and field dependent mobility model is selected. Electrons are accelerated by the electric fields, but

lose momentum as the result of various scattering processes. These scattering mechanisms include lattice vibrations (phonons), impurity ions, other carriers, surfaces, and other material imperfections. Lattice scattering includes acoustic phonon scattering and optical phonon scattering (phonon-electron scattering). Carrier-carrier scattering includes electron-electron scattering. Defect scattering includes surface roughness scattering, crystal defects and impurity-electron scattering. All the effects are described by mobility introduced by the transport model and this mobility is function of local electric field, lattice temperature, doping concentration etc. The equations for Caughey-Thomas doping and field dependent mobility are as follow :

$$\mu_{doping} = \mu_{min} + \frac{\mu^{v}_{max\left(\frac{T}{300}\right)} - \mu_{min}}{1 + \left(\frac{T}{300}\right)^{\xi}\left(\frac{N}{nrefn}\right)^{\alpha}} \tag{1}$$

$$\mu_{field} = \frac{\mu_{doping}}{\left(1 + \left(\frac{\mu_{min\ E}}{v^{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \tag{2}$$

where the user specified quantities are as follow :

i. Minimum Mobility, mu_min (cm/s) : 55.24

ii. Maximum Mobility, mu_max (cm/s) : 1429.23

iii. Exponent Parameter, nu : -2.3

iv. Exponent Parameter, xi : -3.8

v. Exponent Parameter, alpha : 0.73

vi. Reference Impurity Concentration, nrefn : 1.072×10^{17}

vii. Exponent Parameter, beta : 2

viii. Electron Saturation Velocity (cm/s) : 1×10^{7}

ix. Device Temperature : (set to simulation temperatures)

x. Dopant Atom Concentration : (set to body doping concentrations)

xi. Electric Field : (set by drain to source and gate to source voltage)

The ballistic transport using semiclssical approach is solved using Boltzmann Transport Equation (BTE)

$$\frac{\partial f}{\partial t} + \vec{v} \cdot \nabla_r f - \frac{q\vec{E}}{\hbar k}\nabla_k f = \hat{C} f \tag{3}$$

where f is the distribution function of particle, $\vec{E}$ is the electric field, $\hbar k$ is momentum and $\hat{C} f$ is the effects of scattering. In ballistic device, there is no scattering, and $\hat{C} f$ =0.

The ballistic transport using Green's function approach is solved by using the retarded Green's function

$$\mathbf{G} = \left[E\mathbf{I} - \mathbf{H} - \sum_{\text{lead}} \square \right]^{-1} \tag{4}$$

where E is the energy, **H** is discretized Hamiltonian operator matrices and $\sum_{lead}$ is the self energy matrices of boundary conditions.

3. Simulation Results of Temperature Variations at Fixed Device Parameters

In this section, the ambient temperatures of the device are adjusted from 77 K, 100 K, 300 K and 500 K while the other device design parameters remained unchanged. Three separate electron transport models are applied namely, (i) ballistic transport using Green's function approach, (ii) ballistic transport using semiclassical approach, and (iii) drift diffusion transport [5,6]. For drift diffusion transport, Caughey-Thomas doping and field dependent mobility is applied as shown in equation (1) and (2). Also, gate to source voltage (Vgs) is stepped from 0.00 V to 0.60 V with step size 0.10 V. The electrical characteristics studied are 2D electron density along the channel, average electron velocity along the channel and drain current versus gate voltage [7].

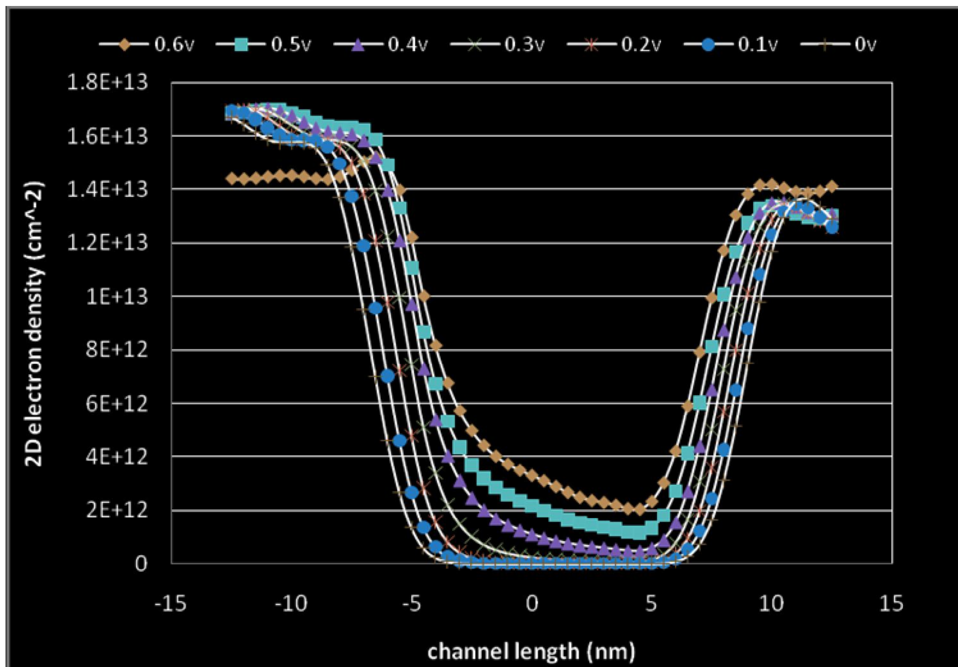

Figure 2: 2D electron density along the channel for various Vgs at 77 K modelled with Ballistic electron transport using Green's function approach.

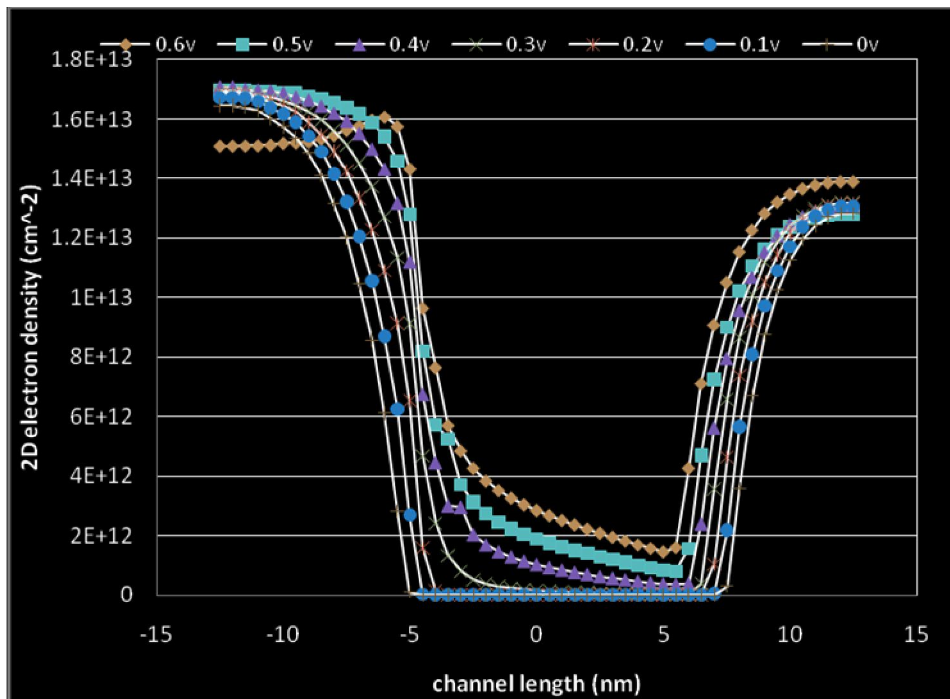

Figure 3: 2D electron density along the channel for various Vgs at 77 K modelled with Ballistic electron transport using semiclassical approach.

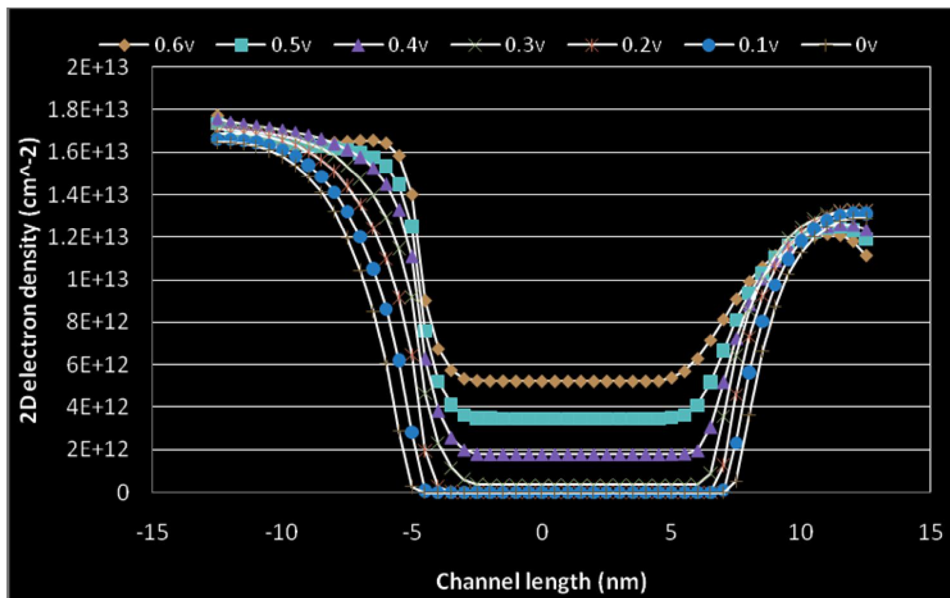

Figure 4: 2D electron density along the channel for various Vgs at 77 K. Drift diffusion electron transport is used.

Figure 2, Figure 3 and Figure 4 shown the plots of 2D electron density along the channel for extremely low temperature condition which is 77 K. Comparing the three plots, the distributions of electron in Silicon channel region is almost flat for drift diffusion transport because at 77 K (extreme low temperature) electron-phonon scatterings are reduced and the lattice vibrations also reduce. In drift diffusion transport model, 2D electron density is almost constant at the channel

region. The gate voltage is varied from 0.00 V, 0.10 V, 0.20 V, 0.30 V, 0.40 V, 0.50 V to 0.60 V. The higher the Vgs, the larger would be the 2D electron density at the channel region. For ballistic transport models, low temperature caused higher potential barrier. But at Vgs=0.60 V, potential barrier is suppressed and so more electron can overcome potential barrier to enter channel region. Drain to source terminal is biased at fixed 0.60 V and so electrons near the drain terminal can enter the drain terminal with high velocity.

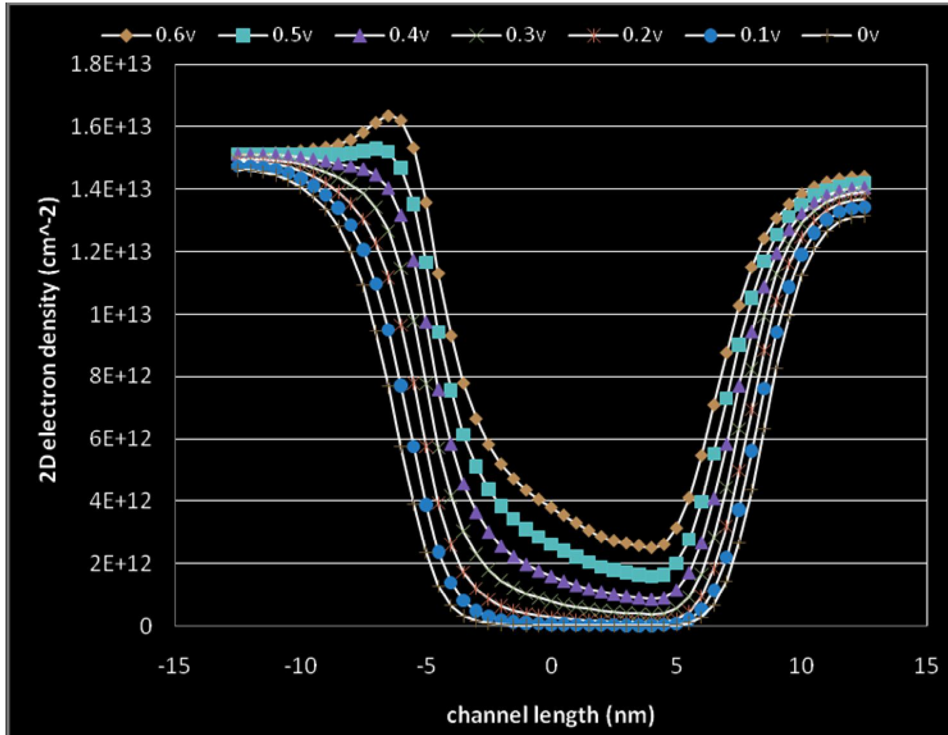

Figure 5: 2D electron density along the channel for various Vgs at 500 K modelled with Ballistic electron transport using Green's function approach.

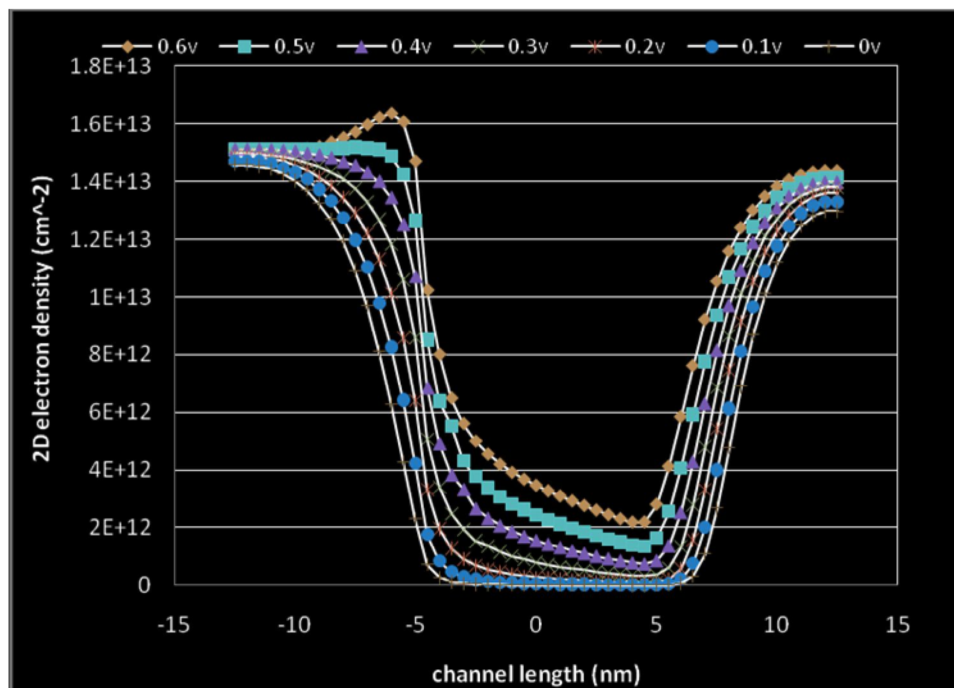

Figure 6: 2D electron density along the channel for various Vgs at 500 K modelled with Ballistic electron transport using semiclassical approach.

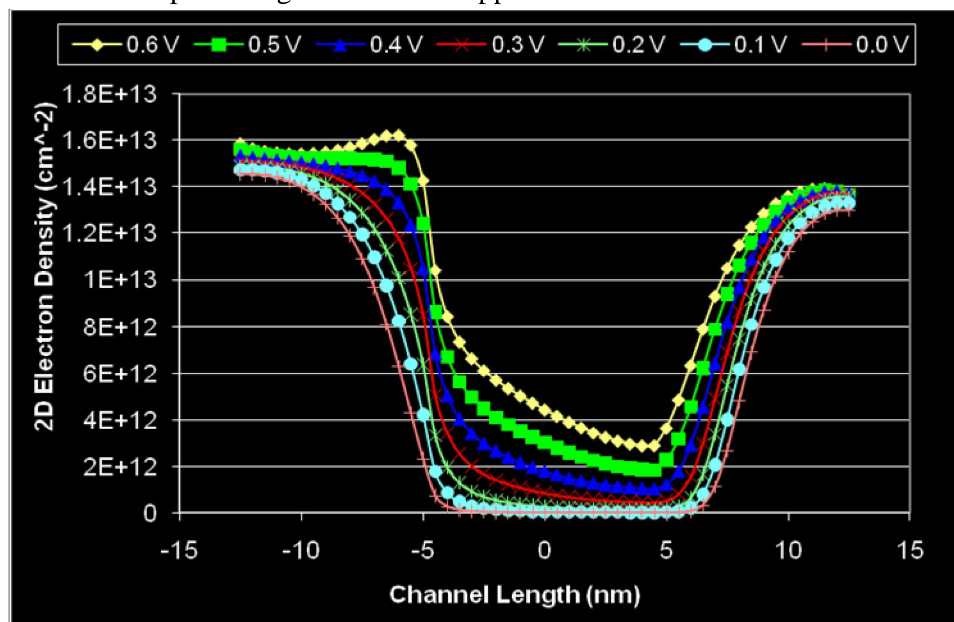

Figure 7: 2D electron density along the channel for various Vgs at 500 K modelled with Drift diffusion electron transport model.

Figure 5, Figure 6 and Figure 7 shown the plots of 2D electron density along the channel for extremely high temperature condition which is 500 K. From these three plots, the 2D electron density profiles in the channel region exhibit higher density near source end than near drain end. For a high drain bias, electron injected from the drain reservoir do not need to be considered. Due to the presence of potential barrier at channel region near the source terminal, electrons need higher potential energy in order to jump across the barrier. Electrons that possess less energy than height

of potential barrier are reflected back. Thus, 2D electron density is higher near source terminal. At channel region near drain terminal, high field region exits because of high drain bias. In this region, electrons are injected to the drain terminal reservoir with high velocity. So, average electron velocity is the highest among the channel length. Also, 2D electron density is low here. From Figure 5, Figure 6 and Figure 7, the higher the gate voltage (Vgs), the larger would be the electron density. At Vgs=0.60 V, the density of electron at the top of the barrier is the highest because of inversion layer density which is controlled by MOS electrostatics capacitor.

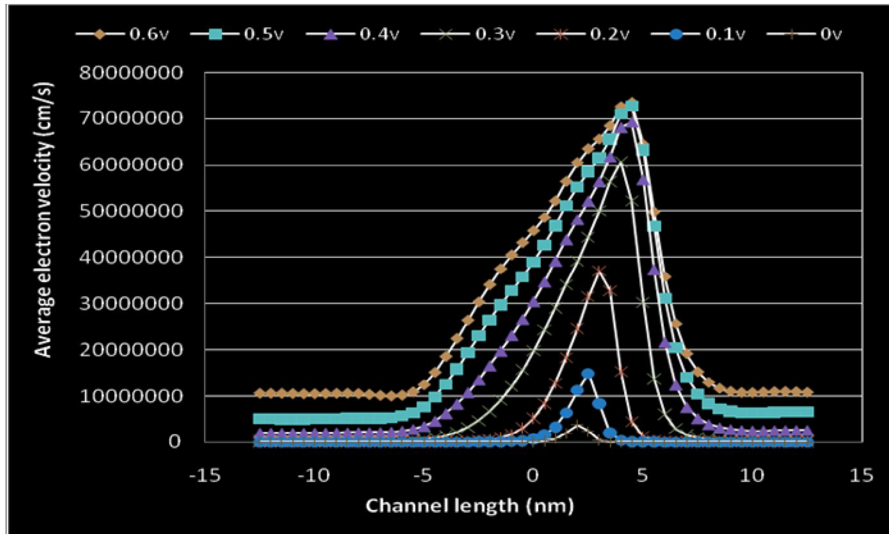

Figure 8: Average electron velocity along the channel for various Vgs at 77 K modelled with Ballistic electron transport using Green’s function approach.

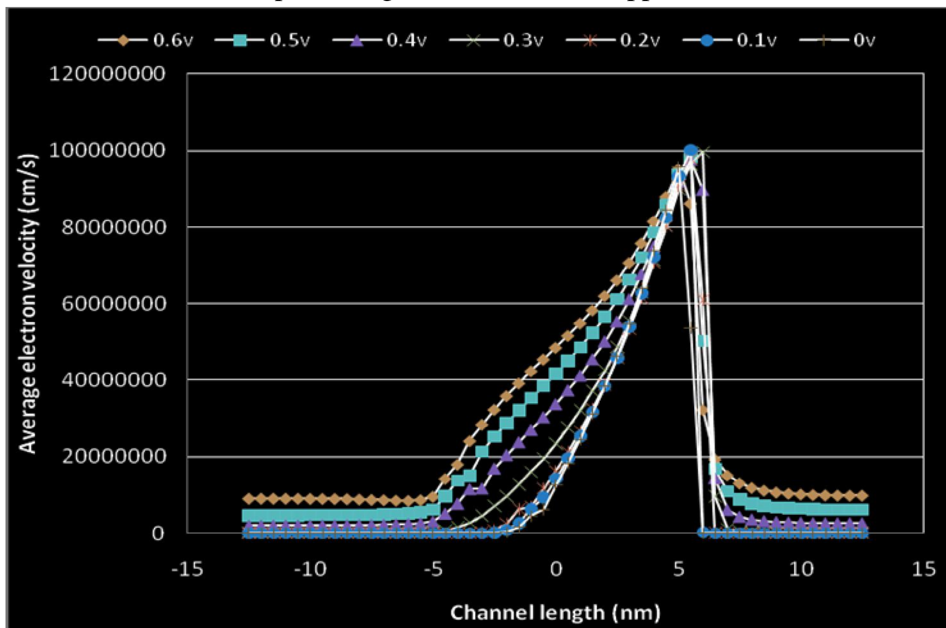

Figure 9: Average electron velocity along the channel for various Vgs at 77 K modelled with Ballistic electron transport using semiclassical approach.

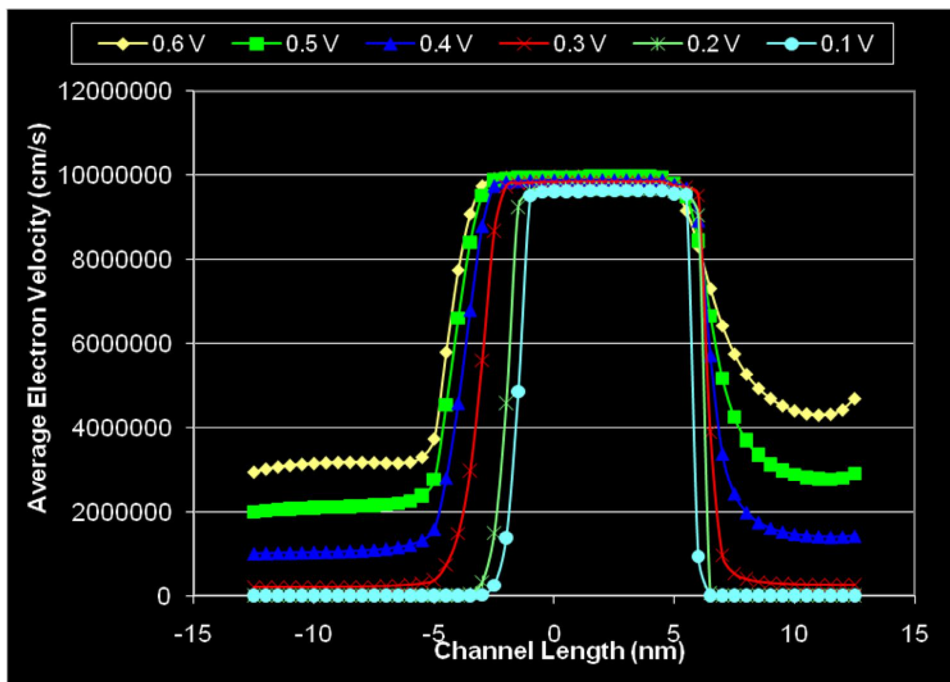

Figure 10: Average electron velocity along the channel for various Vgs at 77 K modelled with Drift diffusion electron transport model.

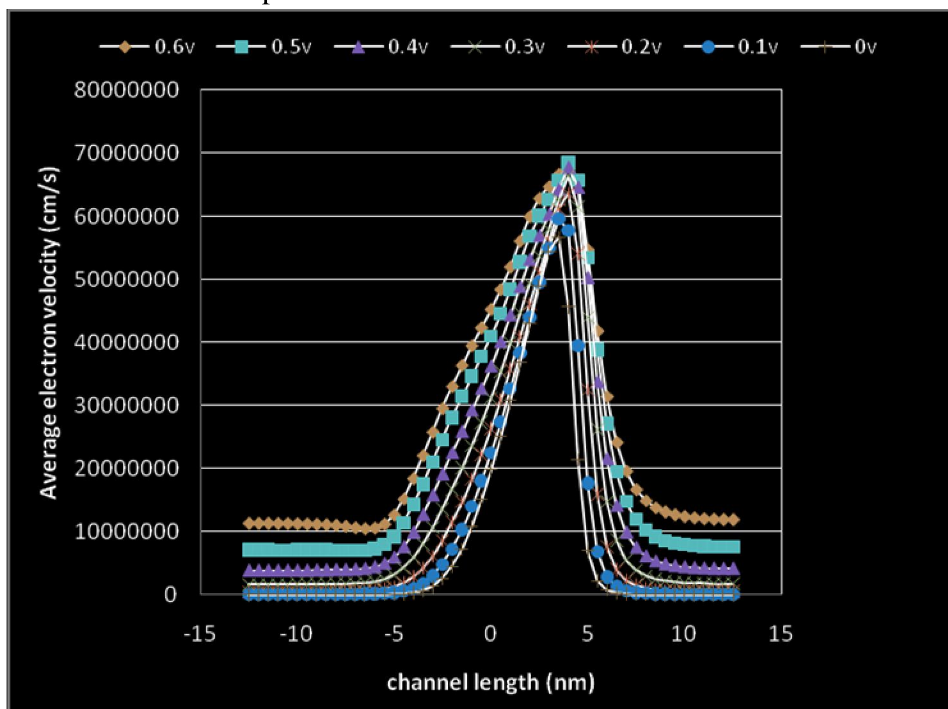

Figure 11: Average electron velocity along the channel for various Vgs at 500 K. Ballistic electron transport using Green's function approach is used.

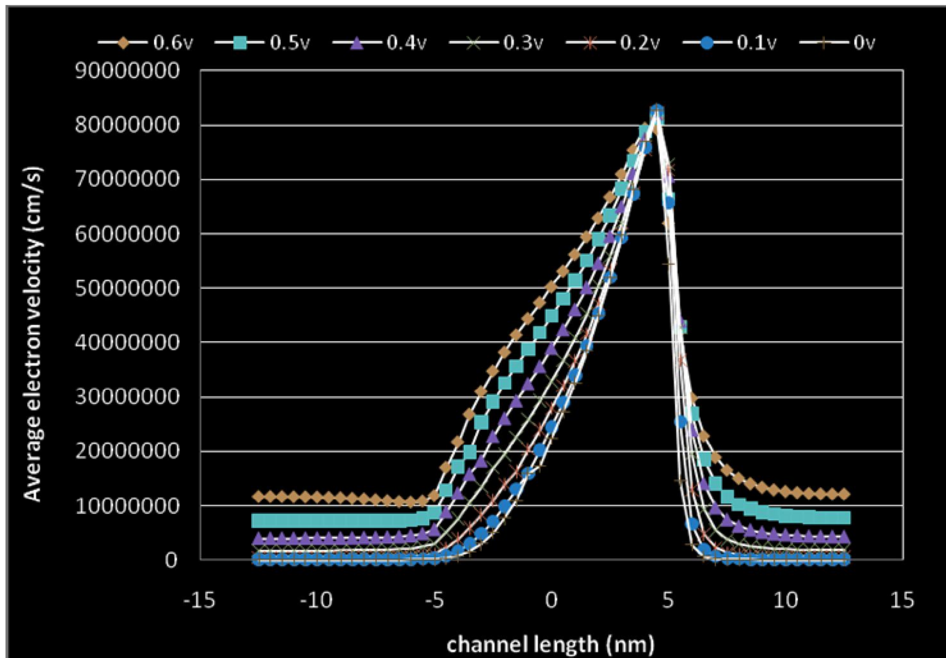

Figure 12: Average electron velocity along the channel for various Vgs at 500 K. Ballistic electron transport using semiclassical approach is used.

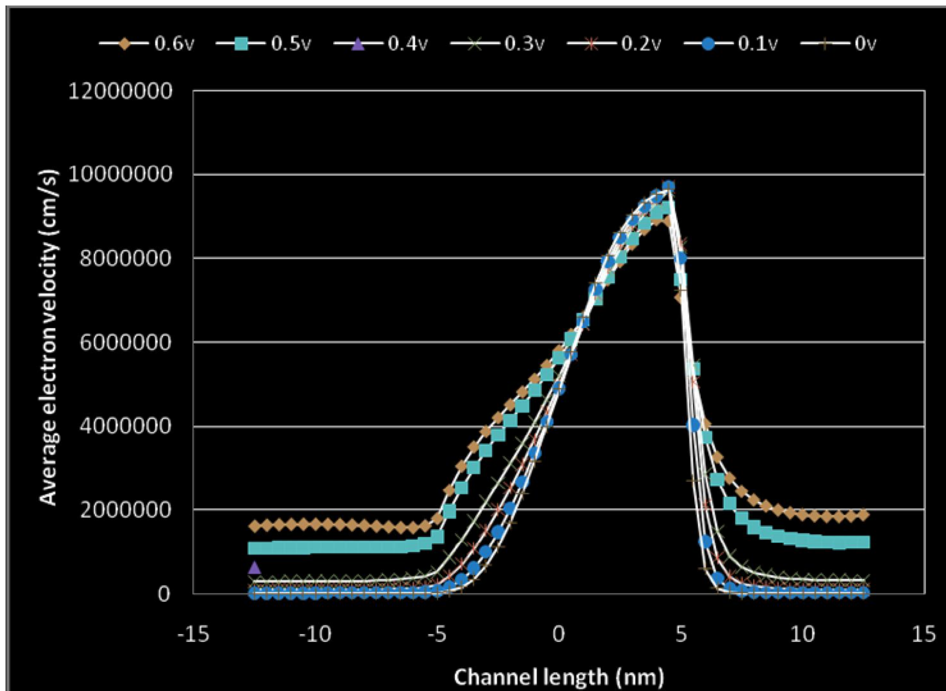

Figure 13: Average electron velocity along the channel for various Vgs at 500 K. Drift diffusion electron transport is used.

At the plots of operating temperature 77 K and 500 K for ballistic electron transport using Green's function approach, electron carriers are treated as wave nature. At 77 K, low gate voltage (Vgs) resulted in low average electron velocity and high gate voltage resulted in high average electron velocity. At the plots of operating temperature 77 K and 500 K for ballistic electron

transport using semiclassical approach, electron carriers are treated as particle nature. The maximum peak value average electron velocity at 77 K is higher than the maximum peak value at 500 K because, at 500 K lattice vibrations increase and this phenomenon hinders the movement of particulate electrons. From the plot of 77 K for drift diffusion transport, the maximum peak value of electron velocity at the channel region remains almost constant at $1x10^7$ cm/s because of reduced electron-phonon scatterings at this low temperature. Overall, the average electron velocity for ballistic transport using Green's function approach and ballistic transport using semiclassical approach is higher than the value for drift diffusion model. So, we expect a lower on-state current (I_{on}) in drift diffusion transport model as proven by graphs for current versus voltage. Because of high electric field near drain terminal, electron transport through the drain end of the channel is rapid (thus highest average electron velocity). As a result, the D.C. current is controlled by how rapidly electrons are transported across a short low field region near the beginning of the channel. This region is the critical, low field "kT-layer".

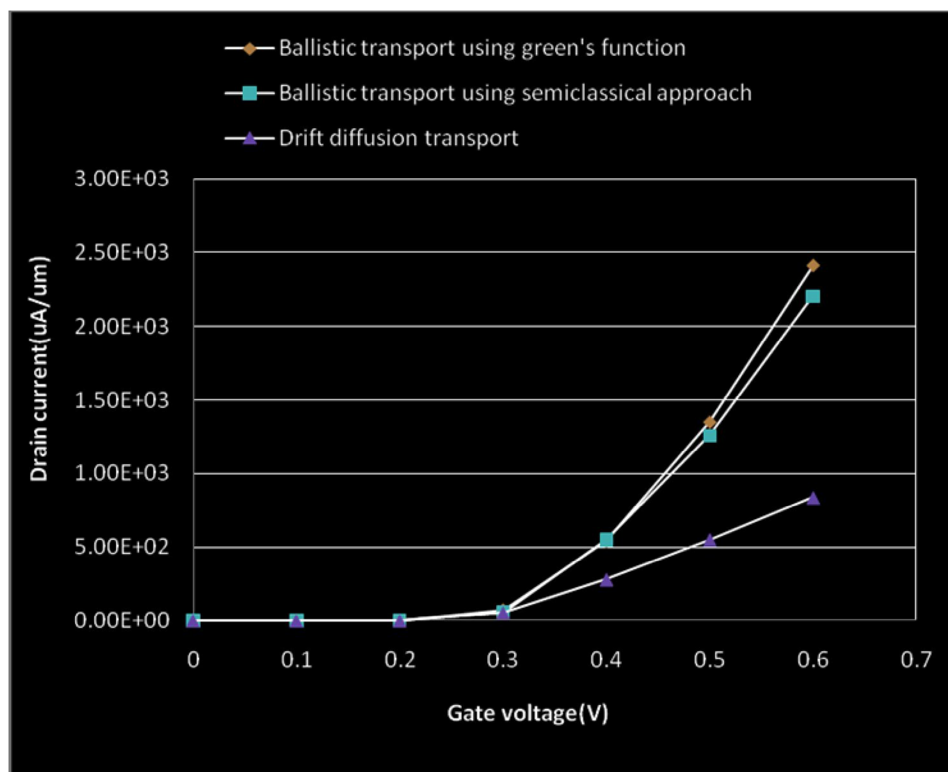

Figure 14: Normal plot of drain current against gate voltage for three different electron transport models at 77 K (extremely low temperature).

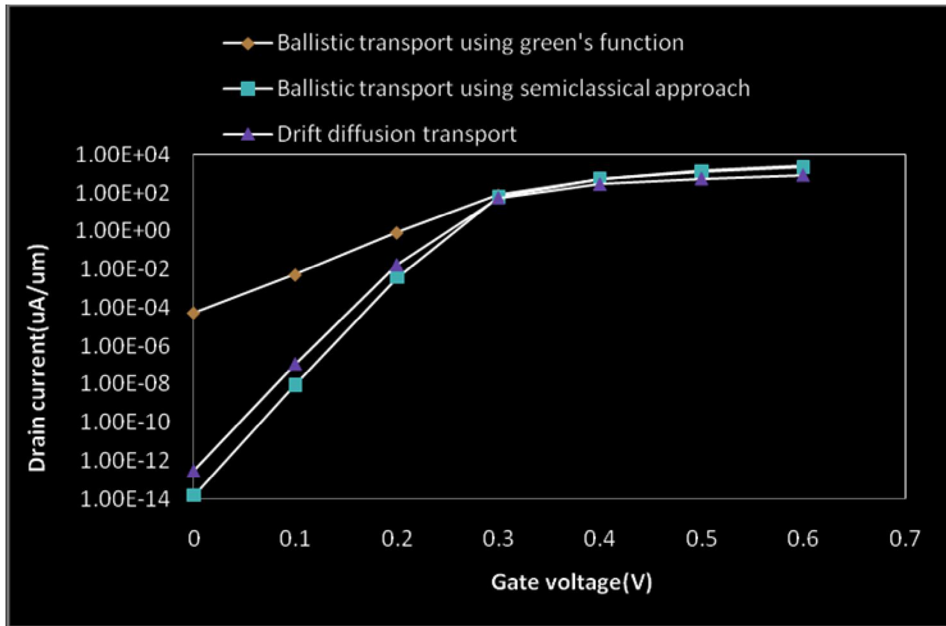

Figure 15: Semilog plot of drain current against gate voltage for three different electron transport models at 77 K (extremely low temperature).

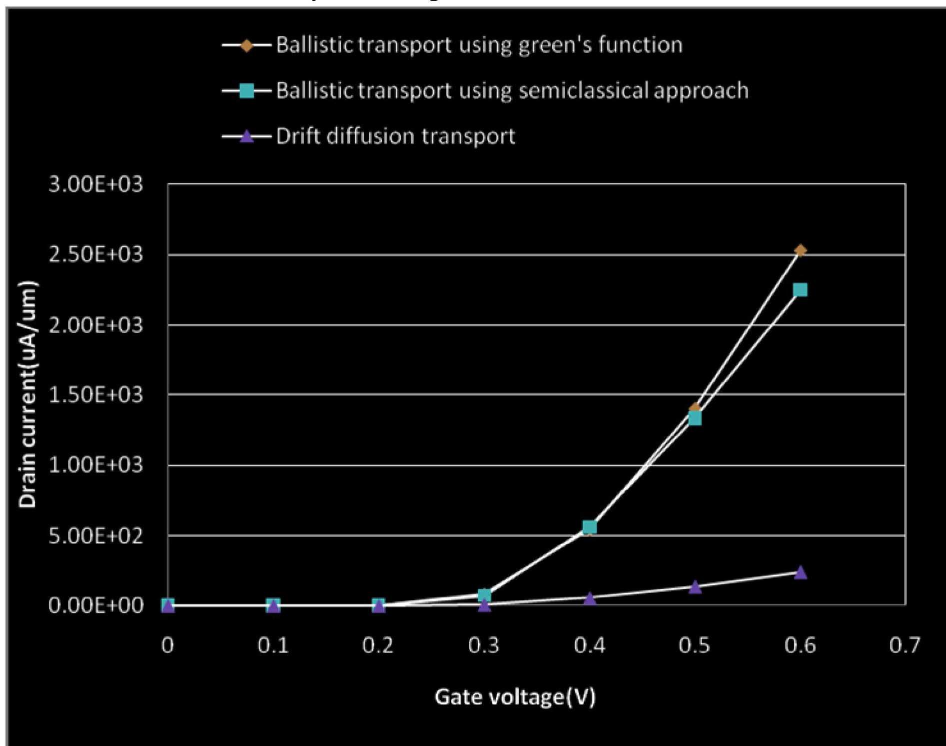

Figure 16: Normal plot of drain current against gate voltage for three different electron transport models at 100 K (extremely low temperature).

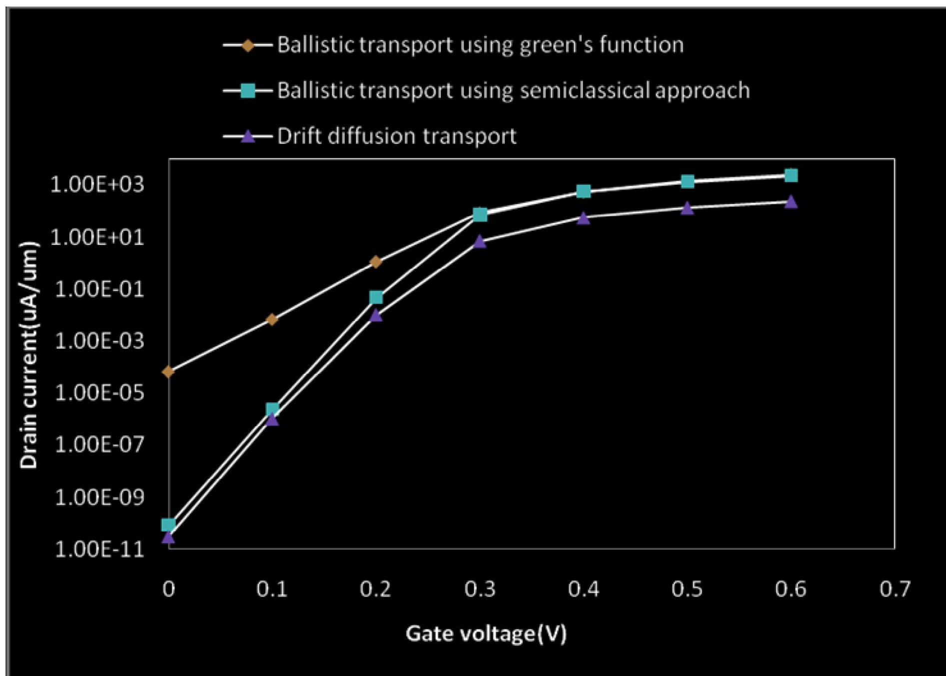

Figure 17: Semilog plot of drain current against gate voltage for three different electron transport models at 100 K (extremely low temperature).

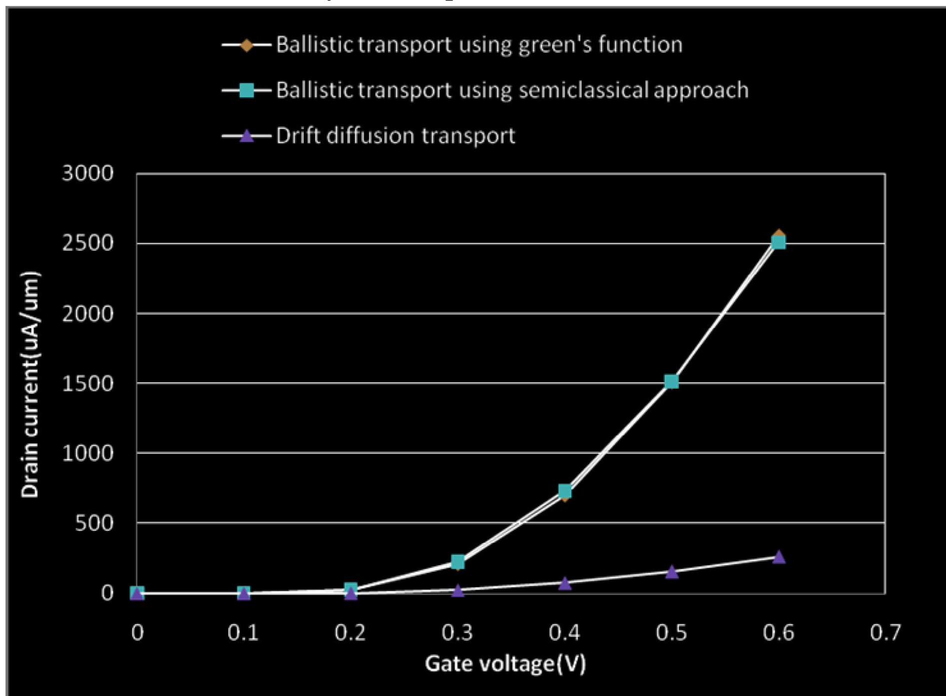

Figure 18: Normal plot of drain current against gate voltage for three different electron transport models at 300 K (room temperature).

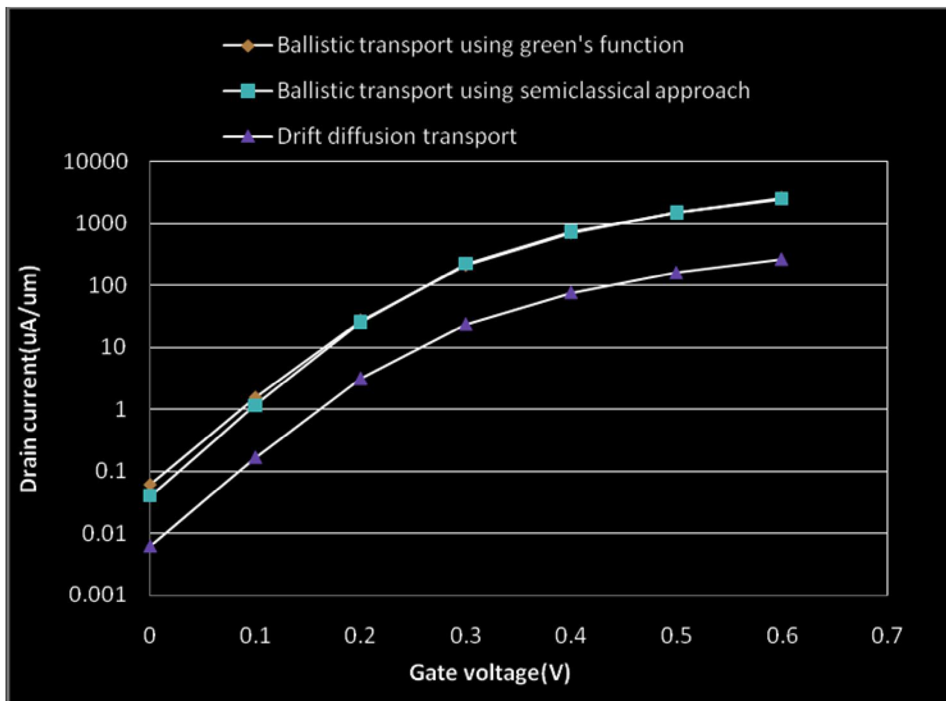

Figure 19: Semilog plot of drain current against gate voltage for three different electron transport models at 300 K (room temperature).

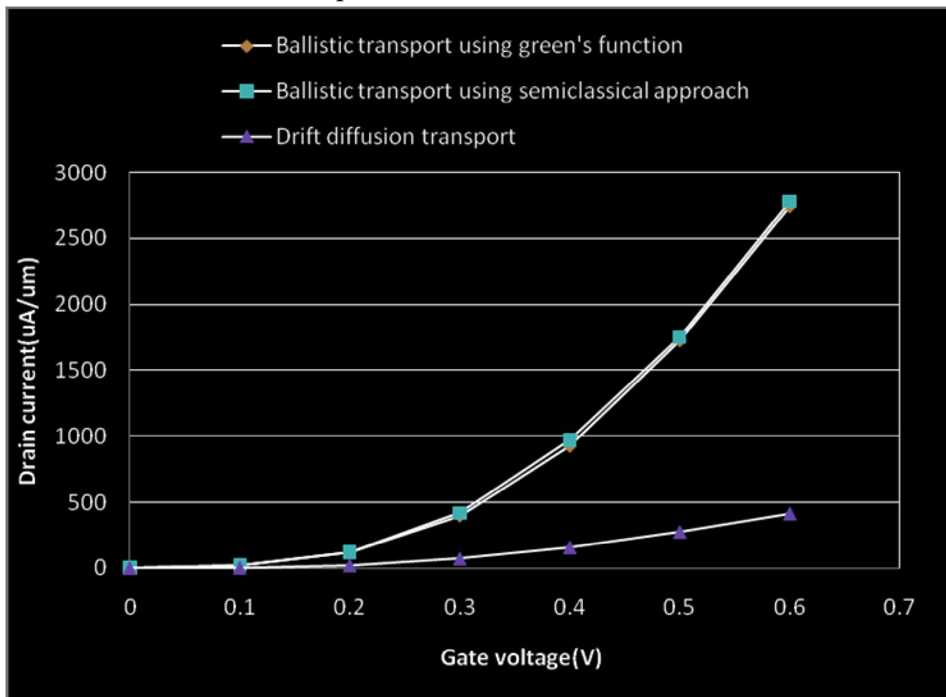

Figure 20: Normal plot of drain current against gate voltage for three different electron transport models at 500 K (extremely high temperature).

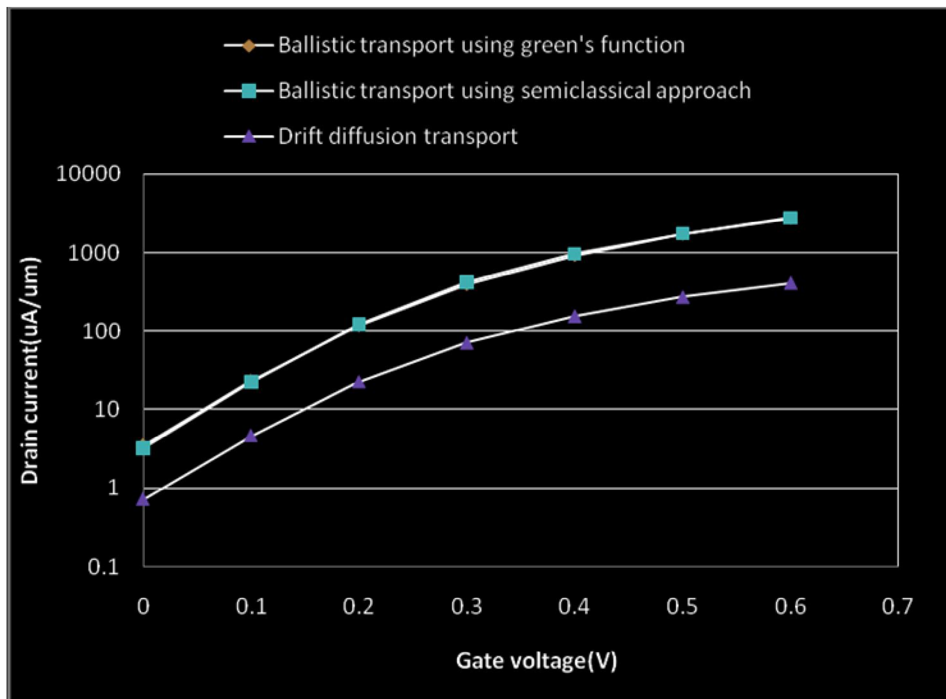

Figure 21: Semilog plot of drain current against gate voltage for three different electron transport models at 500 K (extremely high temperature).

Figure 14 to Figure 21 show the normal as well as semilog plots for drain current versus gate voltage (Id vs Vgs) for three different electron transport models (namely i. Ballistic transport using Green's function, ii. Ballistic transport using semiclassical approach, and iii. Drift diffusion transport) at extremely low temperature (77 K and 100 K), room temperature (300 K) and extremely high temperature (500 K). Mobility model which has been applied when using drift diffusion transport is the Caughey-Thomas doping and field dependent mobility. From those plots, in the cases for ballistic Green's function and ballistic semiclassical approach, the higher the operating temperature, the larger would be the on-state current (I_{on}), the lower would be the threshold voltage (V_{TH}) and the larger would be the leakage current (I_{off}). On the other hand, in the case for drift diffusion transport, the higher the operating temperature, the smaller would be the on-state current (I_{on}) and the larger would be the leakage current (I_{off}). This situation is caused by the fact that when the operating temperature increases, more electron-phonon scattering exist in drift diffusion model which result in reduced mobility and reduced on-state current. From the plots of 77 K and 100 K, leakage current (I_{off}) for ballistic Green's function is higher than ballistic semiclassical approach while for high temperature (500 K), leakage current for these two transport models are roughly equal. This situation is caused by the fact that thermionic emission is included in ballistic transport using semiclassical approach but not in ballistic transport using Green's function.

The off-state current I_{off} is the leakage current when the transistor is off. This leakge current exponentially increases as lattice temperature elevates. The increase in leakage current results in additional power consumption and is not affordable for portable devices, such as mobile phone and laptop computer which rely on battery for their operation. For new trend ultra book, this research

study is potential for thinner device and long battery life. On the aspect of digital elements, switching during logical transition can cause self-heating.

4. Discussion

Electron density becomes zero at the SiO_2/Si interfaces because of quantum effects which consider infinite potential barrier at oxide-silicon interface. Under non-equilibrium operating condition, there is a potential barrier near the source end of the Silicon channel. This barrier height can be modulated by gate voltage. Thus, controlling the number of electrons entering the channel region. As temperature reduces, channel barrier increases, and so less electrons overcome the potential barrier. This phenomenon results in higher source reservoir electron density at low temperature. At gate voltage Vgs=0.6 V, potential barrier is the lowest, thus more electrons can overcome the potential barrier. Therefore, resulting in higher 2D electron density in channel region at high Vgs. At constant Vds=0.6 V, the conduction subbands at source and drain terminal are different with drain terminal at lower values. At higher temperature (500 K), the inversion layer density at the top of potential barrier is roughly equal in the presence or absence of scattering. This situation is a consequence of self-consistent electrostatics and is insensitive to electron transport models. As a result, the 2D electron density distributions are roughly equal for three electron transport models at high temperature.

The temperature variations effects on average electron velocity along the channel length are discussed in this paragraph. Firstly, let focuses on ballistic electron transport using Green's function approach. At low temperature, potential barrier increases, no thermionic effect and low quantum tunnelling at low voltage biasing. So, average electron velocity is low for low voltage biasing. Meanwhile, at high temperature, potential barrier is low and so average electron velocity is large. Secondly, for ballistic electron transport using semiclassical approach, at low temperature, thermal emission is suppressed. So, higher average electron velocity at low temperature. Finally, for drift diffusion transport model at low temperature, electron-phonon scatterings and lattice vibrations are reduced. Since Vds is fixed at constant 0.6 V, there is constant electric field along the channel. So, electron mobility and electron velocity are constant at low temperature. For high temperature, scatterings due to lattice vibrations exist, and so, electron velocity increases linearly from source to drain.

Next, temperature variations effects on current-voltage (I-V) characteristics are discussed in this paragraph. At low temperature, ballistic transport using semiclassical (BTSC) approach has lower leakage current than ballistic transport using Green's function (BTGF) approach because thermionic emission, which is accounted for in BTSC, is low. On the other hand, quantum tunnelling still exists in BTGF at low temperature. At high temperature, thermionic emission is high for BTSC. So, BTGF and BTSC exhibit almost the same high leakage current. The on-state current in drift diffusion is lower than other two transport models because of the existence of scatterings in drift diffusion transport model and the other two models are ballistic in nature.

5. Conclusion

This paper has discussed about the temperature variations effects on the electronic transport properties of double-gate nano-MOSFETs. Low operating temperature and high operating temperature conditions are covered. For low temperature ballistic transport models, semiclassical

approach shows lower leakage current than Green's function approach. On the other side, for high temperature condition, both ballistic transport models exhibit quite similar leakage current. Drift diffusion shows lower on-state current than both ballistic transport models.

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